MODIFICATION OF ELECTRICAL PROPERTIES FOR SEMICONDUCTOR WAFERS

Abstract

A method and structure for fabricating semiconductor wafers. The method comprises providing a plurality of semiconductor wafers. The plurality of semiconductor wafers comprises a first semiconductor wafer and a second semiconductor wafer. The first semiconductor wafer is located adjacent to the second semiconductor wafer. A relationship is provided between a plurality of values for an electrical characteristic and a plurality of materials. A material is chosen from the plurality of materials existing in the relationship. A substructure is formed comprising the material sandwiched between a topside of the first semiconductor wafer and a backside of a portion of the of the second semiconductor wafer. The plurality of semiconductor wafers are placed into a furnace comprising an elevated temperature for processing resulting in a value for the first semiconductor wafer of the electrical characteristic that corresponds to said material in said relationship.